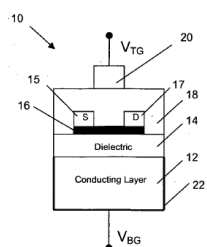


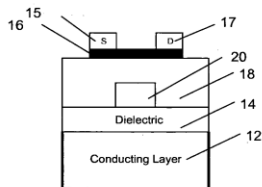
# JOINT DEVELOPMENT OPPORTUNITY

## Graphene Memory Cell and Its Fabrication Methods

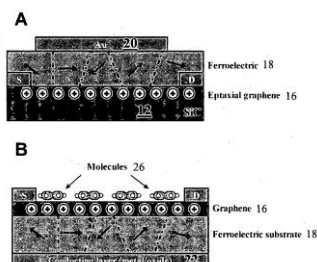
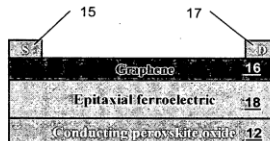
### Various Embodiments of Memory Cell



(a) A basic set up



(b) Alternative arrangements



(c) with electrostatic bias

Ref: Yi Zheng, Guang-Xin Ni, Chee-Tat Toh, Ming-Gang Zeng, Shu-Ting Chen, Kui Yao, and Barbaros Özyilmaz, Applied Physics Letters **94**, 163505, 2009, DOI: [10.1063/1.3119215](https://doi.org/10.1063/1.3119215)

## TECHNOLOGY BACKGROUND

Digital cameras, MP3 players, flash drives, flash cards, smartphones, personal digital assistants (PDAs), portable notebooks and laptops all demand more memory, especially the non-volatile kind. The current technology of high-density, ultra-compact, and low power-consumption storage devices has seen off the days of bulky hard disk drives. Examples of such non-volatile devices include NAND flash memories and ferroelectric RAM (FeRAM). NAND memory has a silicon metal-oxide-semiconductor field-effect transistor (Si MOSFET) with a floating gate and a control gate. Ferroelectric RAM utilizes ferroelectric capacitors for data storage.

Non-volatile device	Advantages	Disadvantages
NAND Flash Memory	Faster speed and more compact structure compared with hard disk drives; simple circuit design; fast increasing capacity (due to aggressive scalability)	Slow random access time; limited write-erase-cycles; necessity of block erasure; high voltages needed for writing and erasing processes
FeRAM	Needs only a marginally higher writing voltage than the reading voltage; both read and write can be done in bit-by-bit fashion; less power needed than NAND; more balanced read and write operation; much faster than NAND	Reading process of '1' state is destructive; a following re-writing process required to get the state back to '1'; scalability is unclear.

## DETAILS OF INVENTION

- The invention is basically a memory cell that has graphene as the working medium: graphene between ferroelectric and dielectric layers, on a flexible, conducting and/or transparent substrate. Switching the graphene using known gate dielectrics gives a volatile operation. Switching using a ferroelectric layer as the gate dielectric gives a non-volatile operation.
- The graphene layer has controllable resistance states representing memory cell data values.
- A ferroelectric layer that is configured can be added to control the resistance states.
- A top electrode can be electrically coupled to the ferroelectric layer in which the graphene layer is at: (1) high resistance state under ferroelectric depolarization and (2) low resistance state under ferroelectric polarization.
- Graphene may be derived from graphene oxide, chemically modified graphene, i.e. graphene, growth by CVD, low pressure CVD, or plasma-enhanced CVD on copper, nickel or cobalt, or mechanically exfoliated from bulk graphite. It may be in one, two, three or more layers in the form of a pristine 2D sheet, or patterned into nanoscale dimensions of dots, dot arrays, nanowires, or nanowire arrays. An intrinsic energy band structure may be in place or one is engineered by lateral confinement, strain stress or electric field.

## APPLICATION AREAS

- Cost-effective flexible, transparent electronic devices;
- Ultra-fast reading & writing memories using symmetric and asymmetric strategies

## BENEFITS OFFERED

- Memory cell with low bias writing and reading process
- Versatility of multilayer stack of graphene and ferroelectric gates – a 3D memory architecture
- Low power consumption with high reliability
- Data readings are not destructive, avoiding re-writing.
- Switching time is increased; power usage reduced.
- High speed reading speeds as fast as the current DRAM
- Field-dependent conductivity provided by graphene
- Reading of stored values is just detecting the (tunable) graphene layer resistance
- Both inorganic and organic materials may be used for the ferroelectric gate.

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